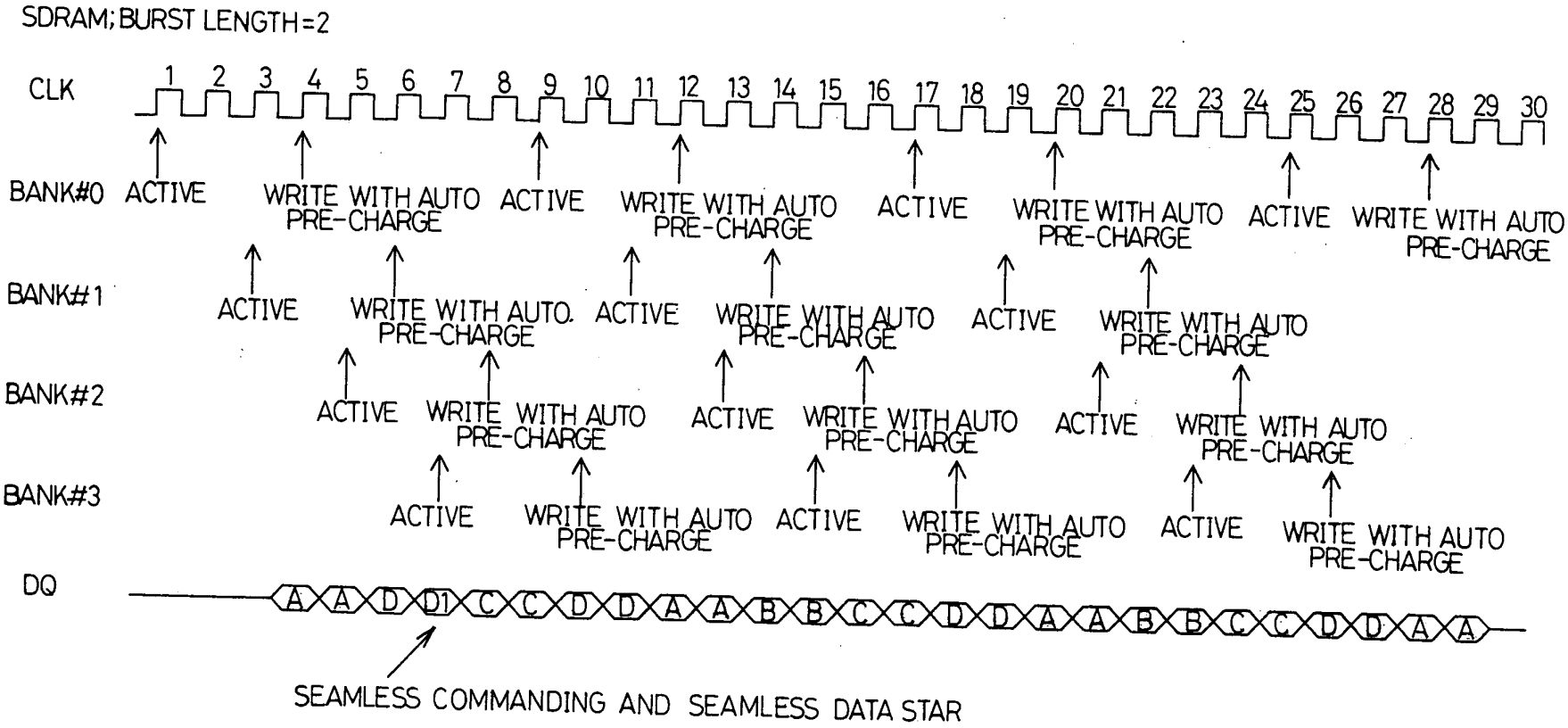

FIG.1A

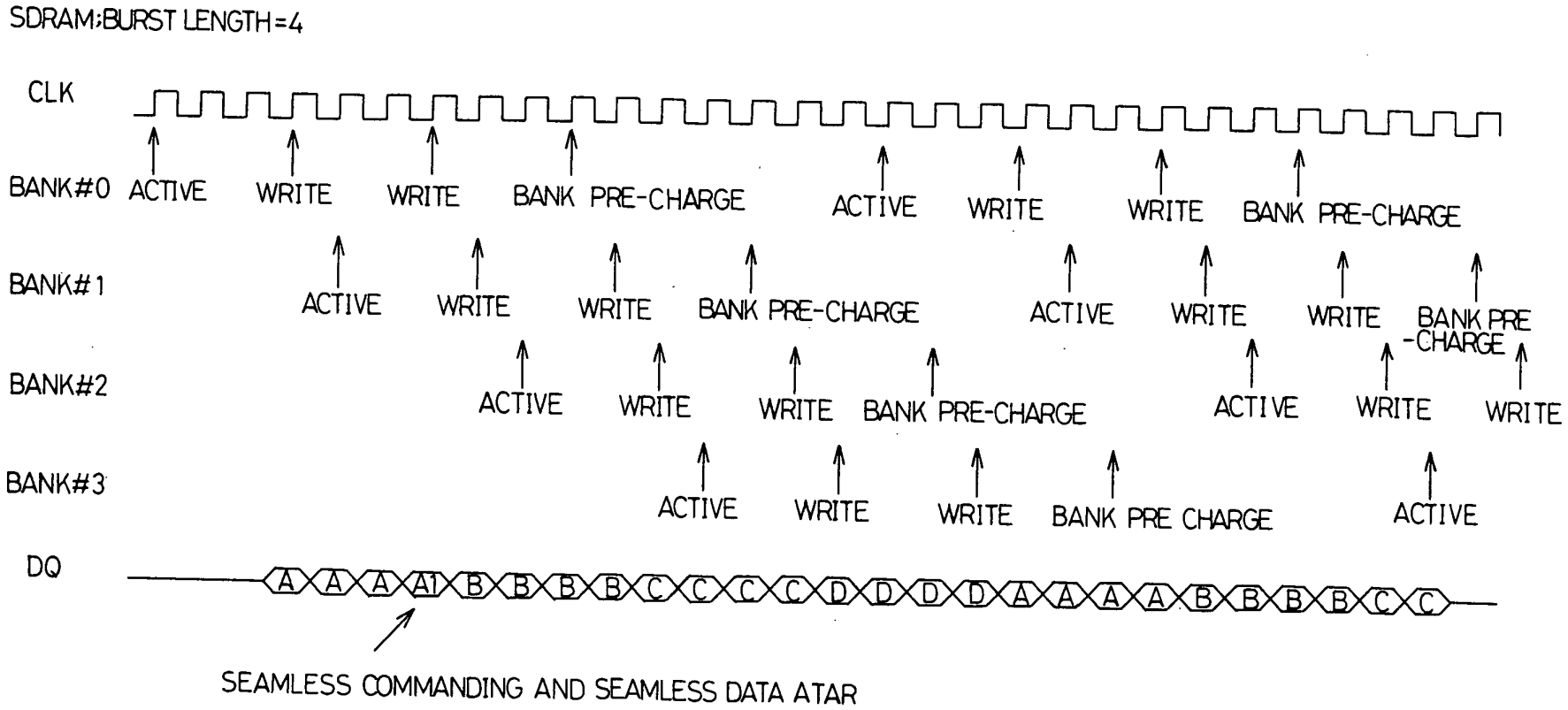

FIG.1B

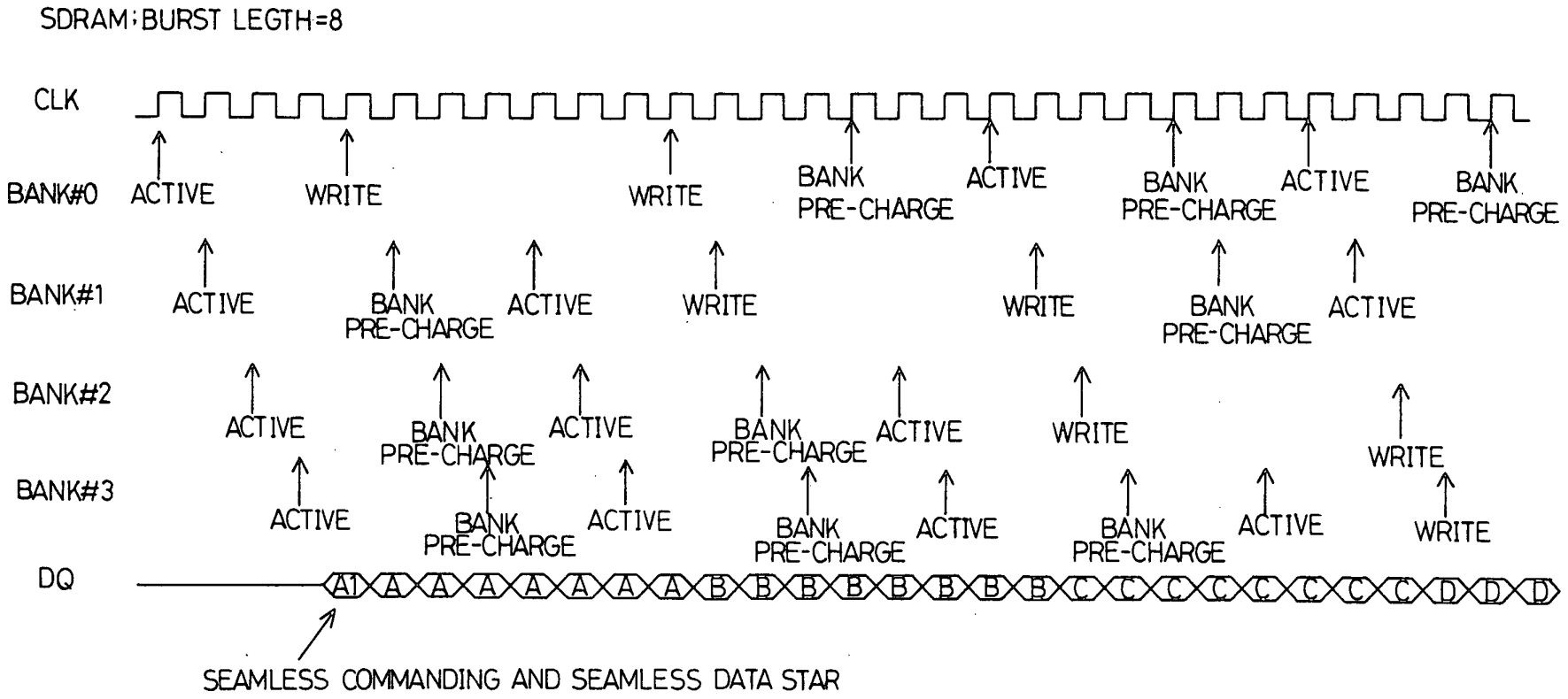

FIG.1C

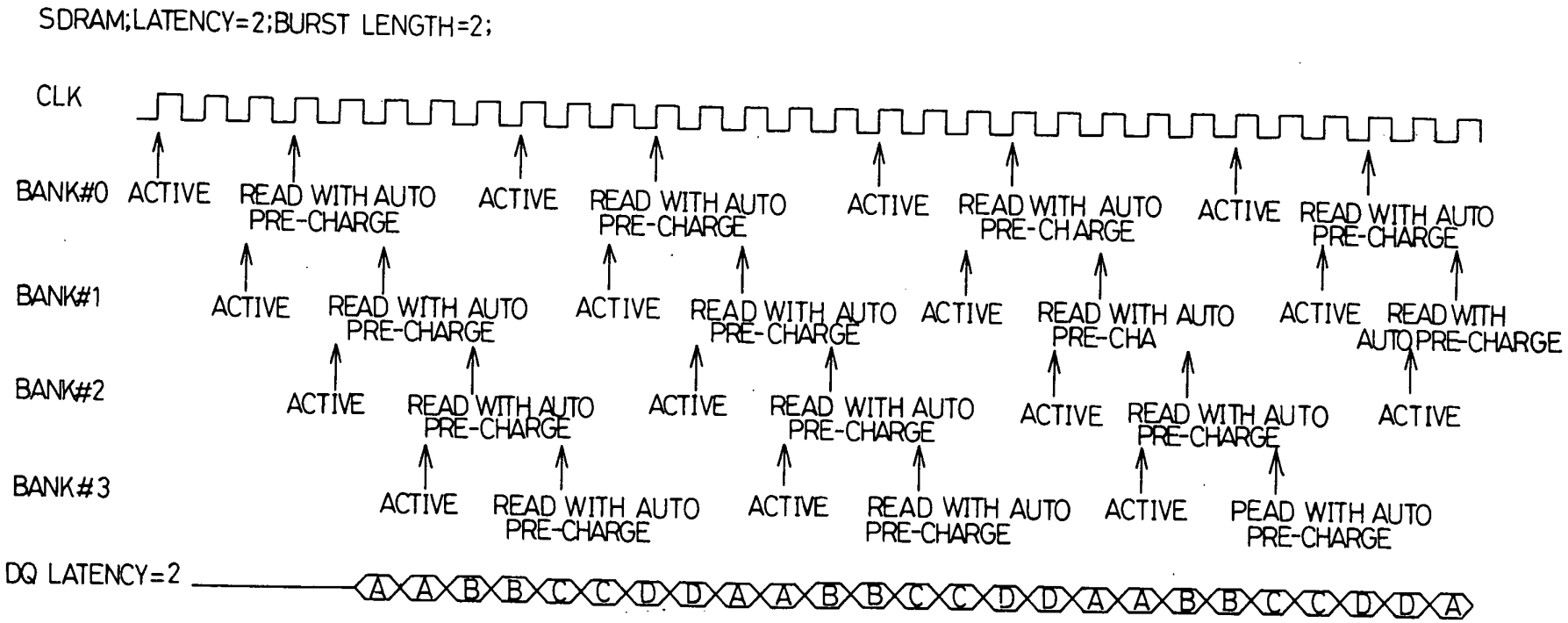
SDRAM;LATENCY=2;BURST LENGTH=2;
CLK
BANK#0
BANK#1
BANK#2
BANK#3
DQ LATENCY=2
ACTIVE
READ WITH AUTO PRE-CHARGE
A A B B C C D D A A B B C C D D A A B B C C D D A

FIG. 2A

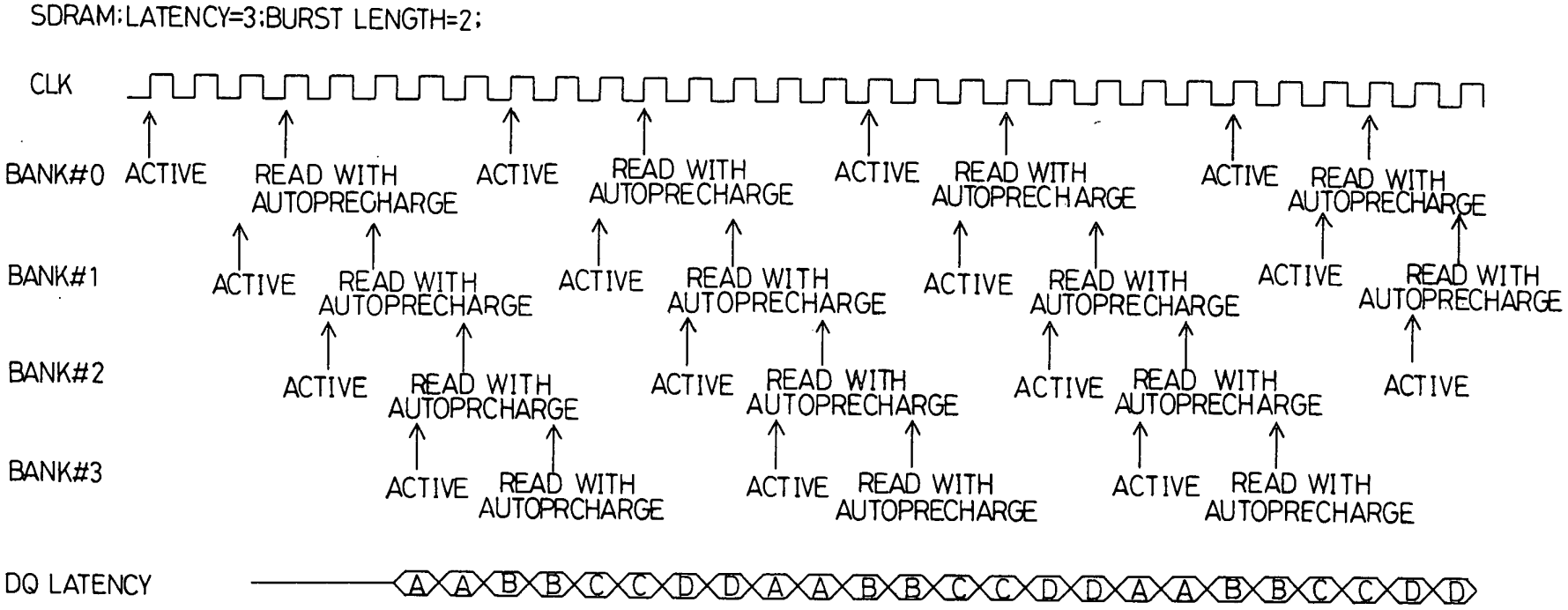
SDRAM:LATENCY=3:BURST LENGTH=2;
CLK
BANK#0
BANK#1
BANK#2
BANK#3
DQ LATENCY
ACTIVE
READ WITH AUTOPRECHARGE
READ WITH AUTOPRCHARGE
A A B B C C D D A A B B C C D D A A B B C C D D

FIG. 2B

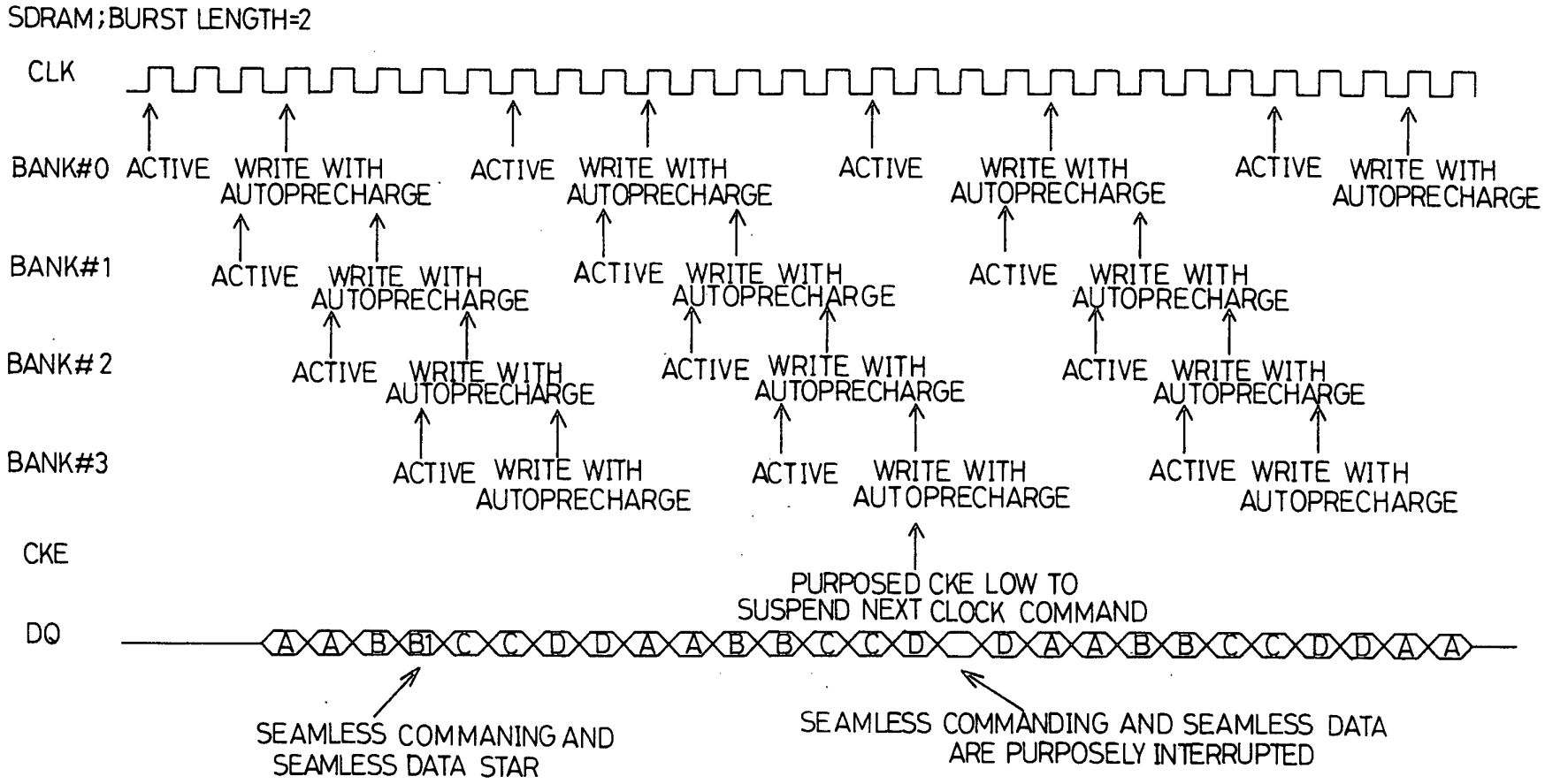
SDRAM;BURST LENGTH=2
CLK
BANK#0
BANK#1
BANK#2
BANK#3
CKE
DQ
ACTIVE
WRITE WITH AUTOPRECHARGE
PURPOSED CKE LOW TO SUSPEND NEXT CLOCK COMMAND
SEAMLESS COMMANING AND SEAMLESS DATA STAR
SEAMLESS COMMANDING AND SEAMLESS DATA ARE PURPOSELY INTERRUPTED

FIG.2C

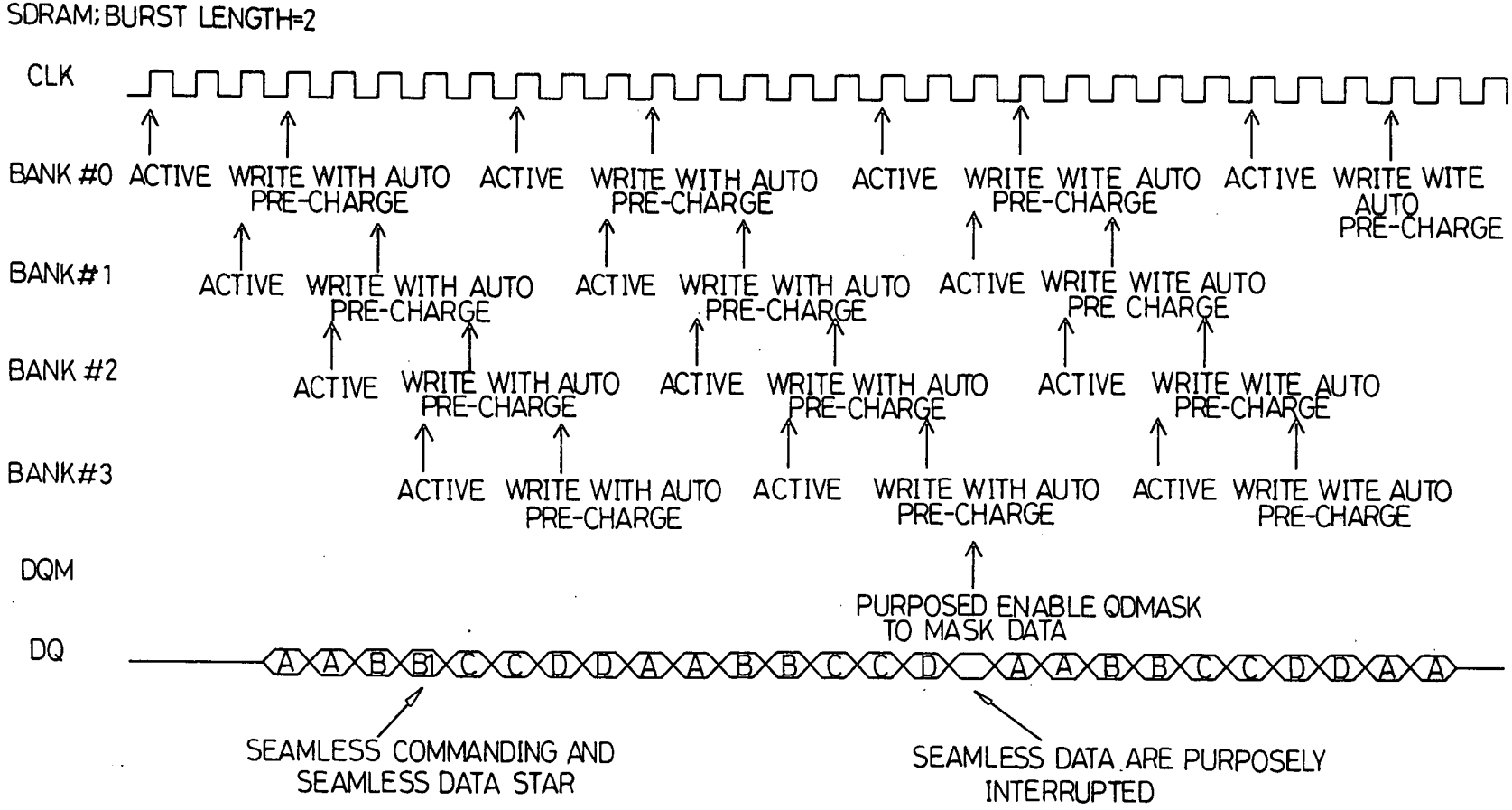
SDRAM; BURST LENGTH=2
CLK
BANK #0
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACTIVE
WRITE WITE AUTO PRE-CHARGE
ACTIVE
WRITE WITE AUTO PRE-CHARGE
BANK #1
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACTIVE
WRITE WITE AUTO PRE CHARGE
BANK #2
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACTIVE
WRITE WITE AUTO PRE-CHARGE
BANK #3
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACTIVE
WRITE WITE AUTO PRE-CHARGE
DQM
PURPOSED ENABLE QDMASK TO MASK DATA
DQ
A A B B C C D D A A B B C C D A A B B C C D D A A
SEAMLESS COMMANDING AND SEAMLESS DATA STAR
SEAMLESS DATA ARE PURPOSELY INTERRUPTED

FIG. 2D

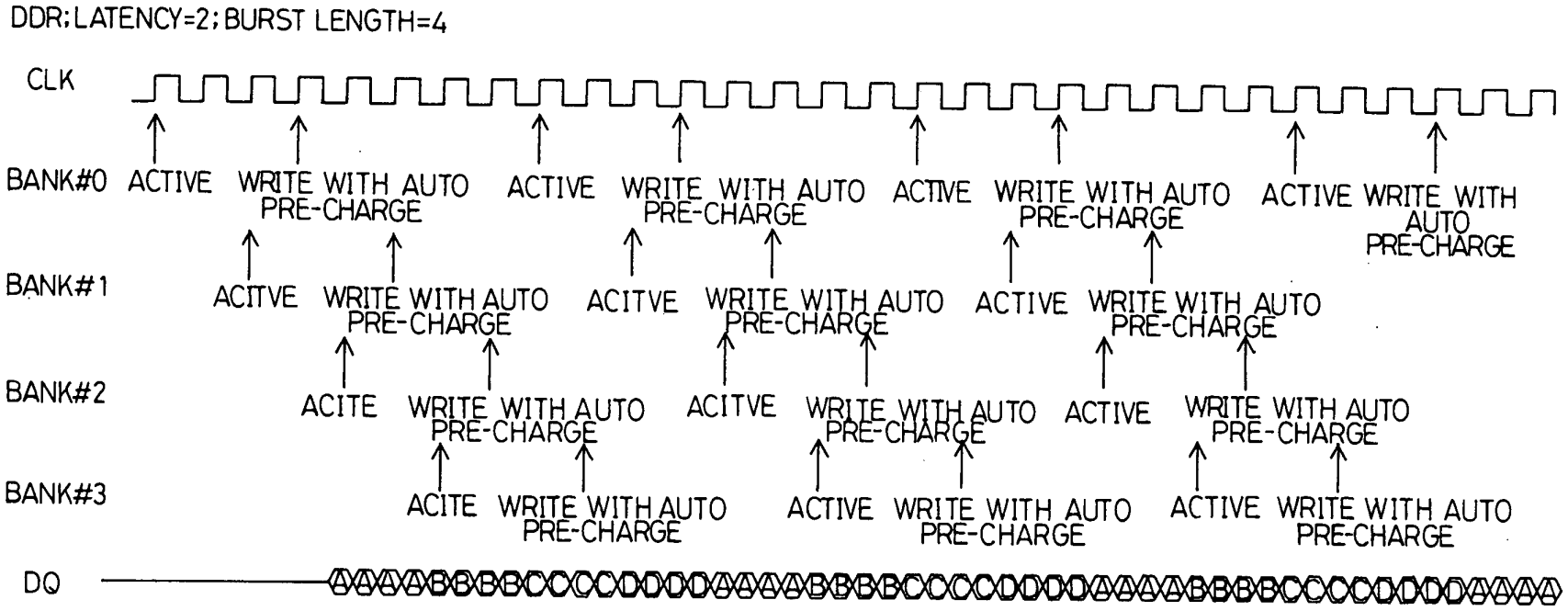
DDR; LATENCY=2; BURST LENGTH=4
CLK
BANK#0
BANK#1
BANK#2
BANK#3
DQ
ACTIVE
WRITE WITH AUTO PRE-CHARGE
ACITVE
ACITE
ACTIVE

FIG.3A

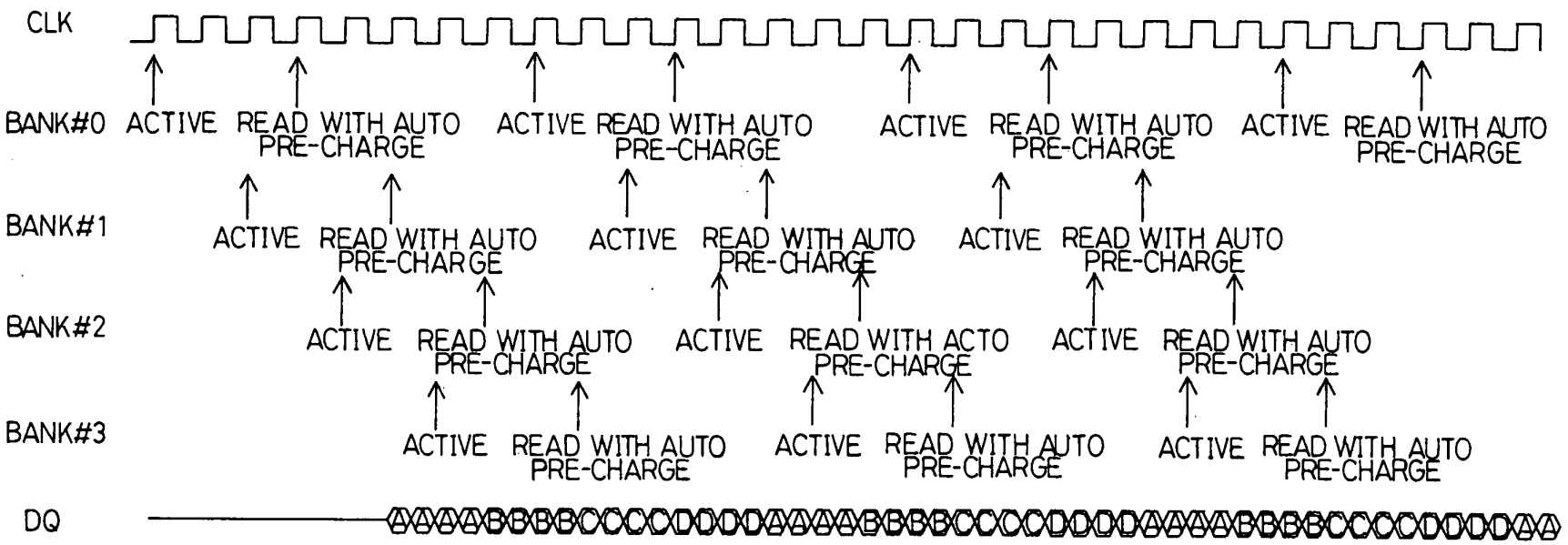
DDR: LATENCY=2; BURST LENGTH=4
CLK
BANK#0
BANK#1
BANK#2
BANK#3
DQ
ACTIVE
READ WITH AUTO PRE-CHARGE
READ WITH ACTO PRE-CHARGE

FIG.3B

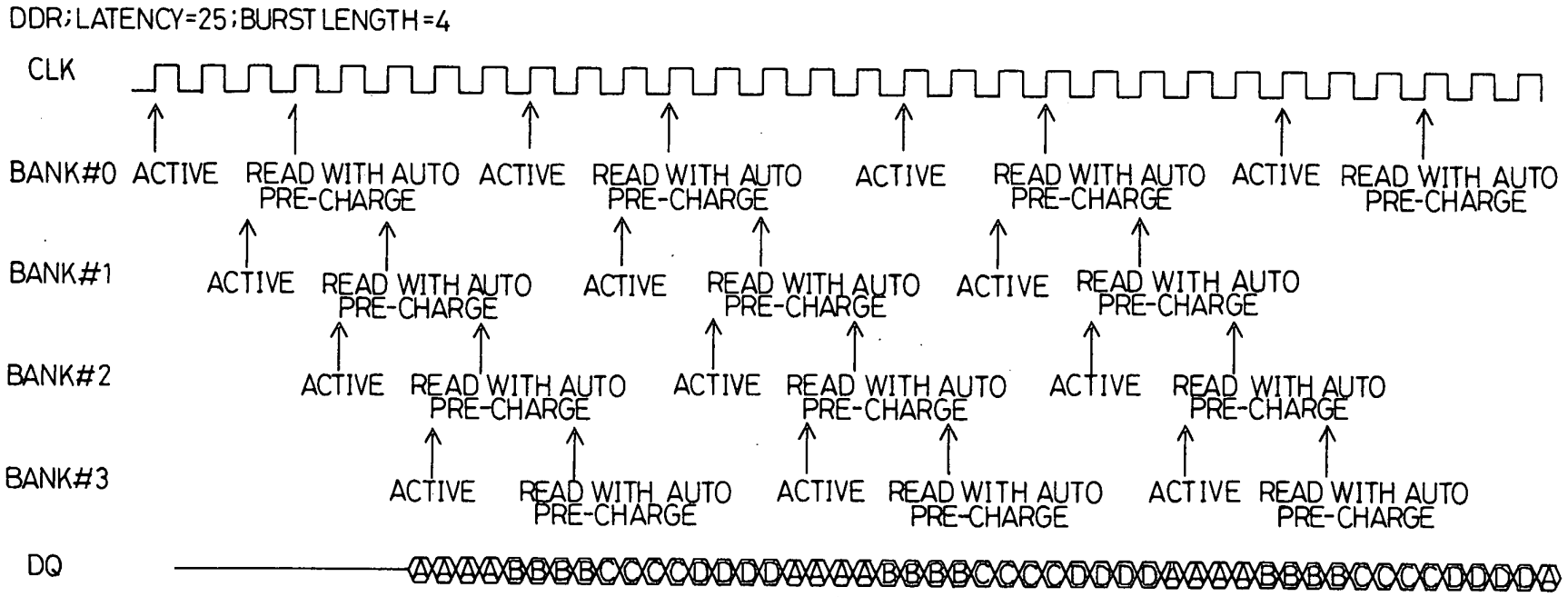
DDR; LATENCY=25; BURST LENGTH=4
CLK
BANK#0
BANK#1
BANK#2
BANK#3
DQ
ACTIVE
READ WITH AUTO PRE-CHARGE

FIG. 3C

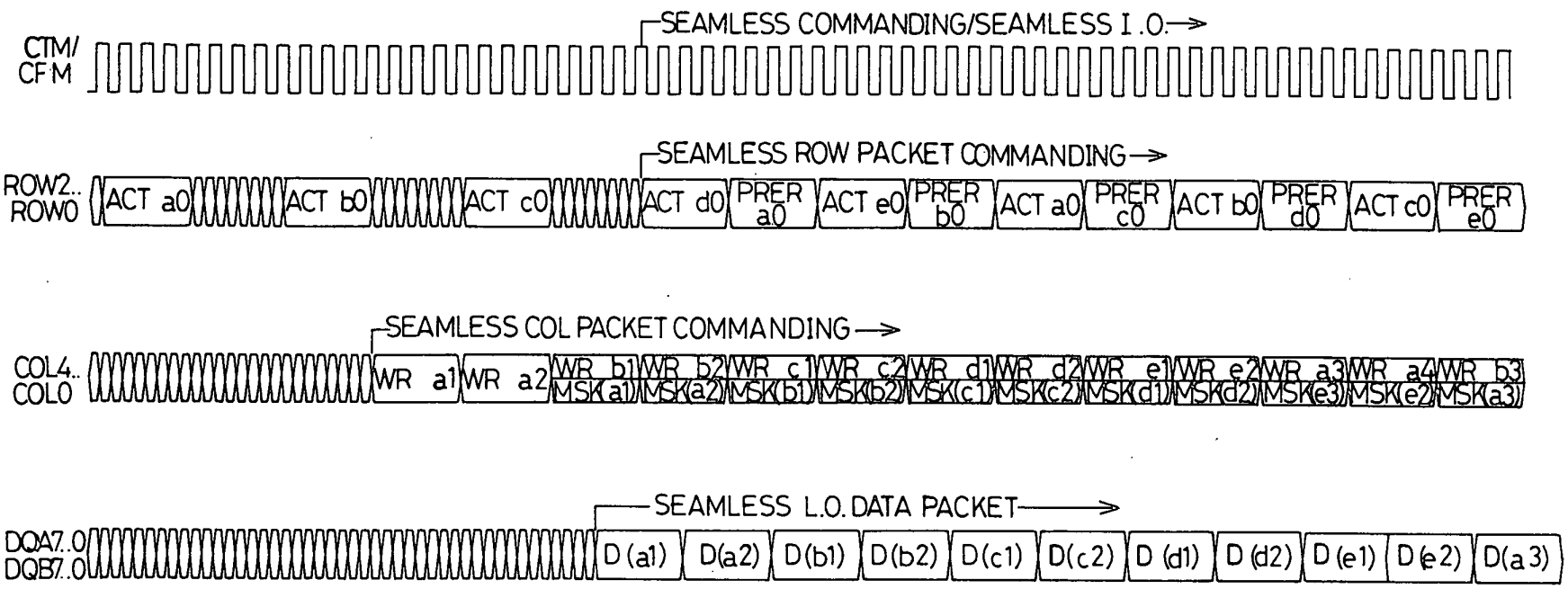
RDRAM: TRR=8 TCYCLE; TCWD=6 TCYCLE; TRTP=4 TCYCLE;
SEAMLESS COMMANDING/SEAMLESS I.O.→
CTM/
CFM
SEAMLESS ROW PACKET COMMANDING→
ROW2..
ROW0
ACT a0
ACT b0
ACT c0
ACT d0
PRER a0
ACT e0
PRER b0
ACT a0
PRER c0
ACT b0
PRER d0
ACT c0
PRER e0
SEAMLESS COL PACKET COMMANDING→
COL4..
COL0
WR a1
WR a2
WR b1
WR b2
WR c1
WR c2
WR d1
WR d2
WR e1
WR e2
WR a3
WR a4
WR b3
MSK(a1)
MSK(a2)
MSK(b1)
MSK(b2)
MSK(c1)
MSK(c2)
MSK(d1)
MSK(d2)
MSK(e3)
MSK(e2)
MSK(a3)
SEAMLESS L.O. DATA PACKET→
DQA7..0
DQB7..0
D(a1)
D(a2)
D(b1)
D(b2)
D(c1)
D(c2)
D(d1)
D(d2)
D(e1)
D(e2)
D(a3)

FIG. 4A

TRANSACTION A:	a0={Da,Ba,Ra0}	a1={Da,Ba,Ca1}	a2={Da,Ba,Ca2}	a3={Da,Ba,Ca3}	a4={Da,Ba,Ca4}
TRANSACTION B:	b0={Db,Bb,Rb0}	b1={Db,Bb,Cb1}	b2={Db,Bb,Cb2}	b3={Db,Bb,Cb3}	b4={Db,Bb,Cb4}
TRANSACTION C:	c0={Dc,Bc,Rc0}	c1={Dc,Bc,Cc1}	c2={Dc,Bc,Cc2}	c3={Dc,Bc,Cc3}	c4={Dc,Bc,Cc4}
TRANSACTION D:	d0={Dd,Bd,Rd0}	d1={Dd,Bd,Cd1}	d2={Dd,Bd,Cd2}	d3={Dd,Bd,Cd3}	d4={Dd,Bd,Cd4}
TRANSACTION E:	e0={De,Be,Re0}	e1={De,Be,Ce1}	e2={De,Be,Ce2}	e3={De,Be,Ce3}	e4={De,Be,Ce4}

RDRAM: TRR=8 TCYCLE; TCAC=8 TCYCLE; TRAS=20 TCYCLE; TRDP=4 TCYCLE;

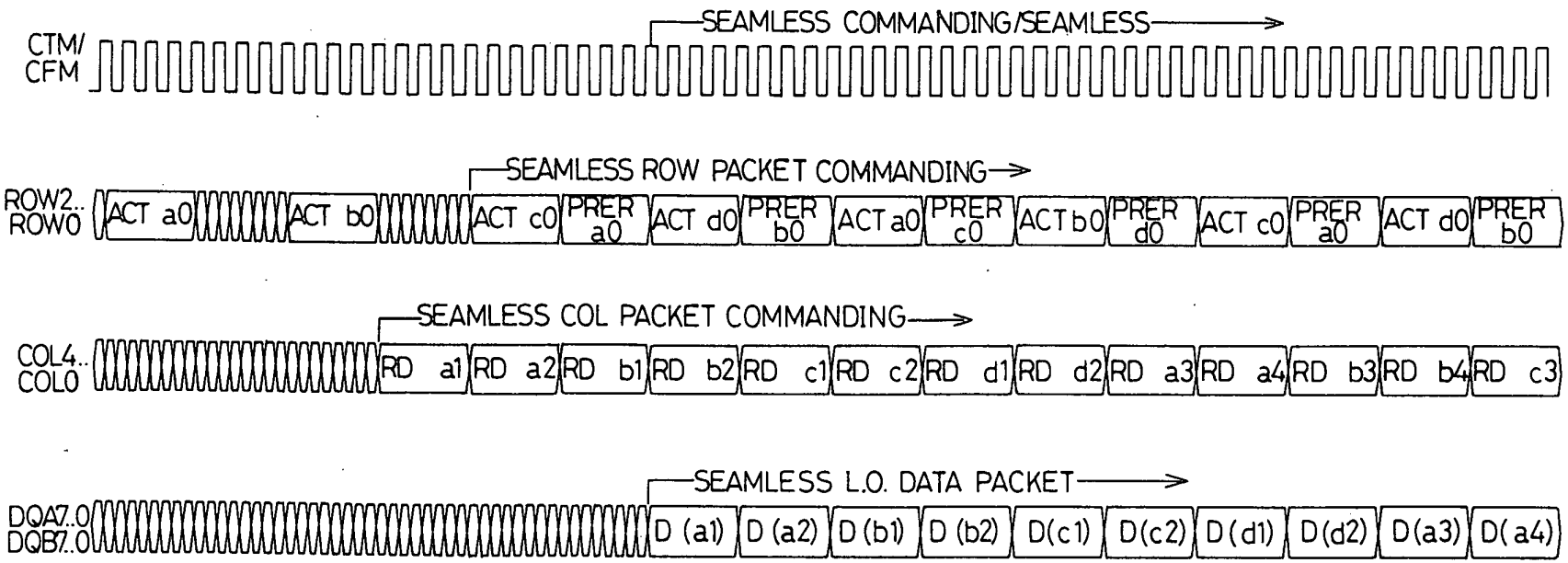

FIG.4B

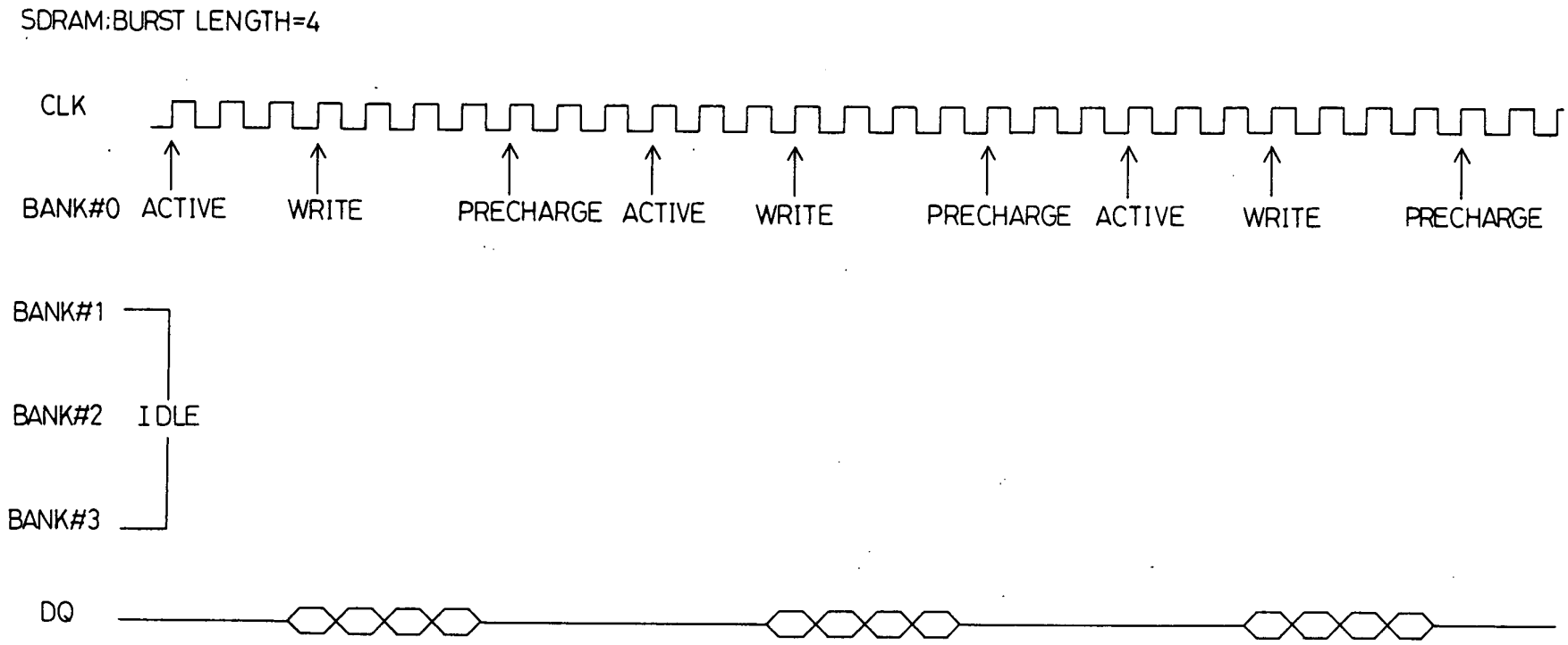

FIG.5
PRIOR ART

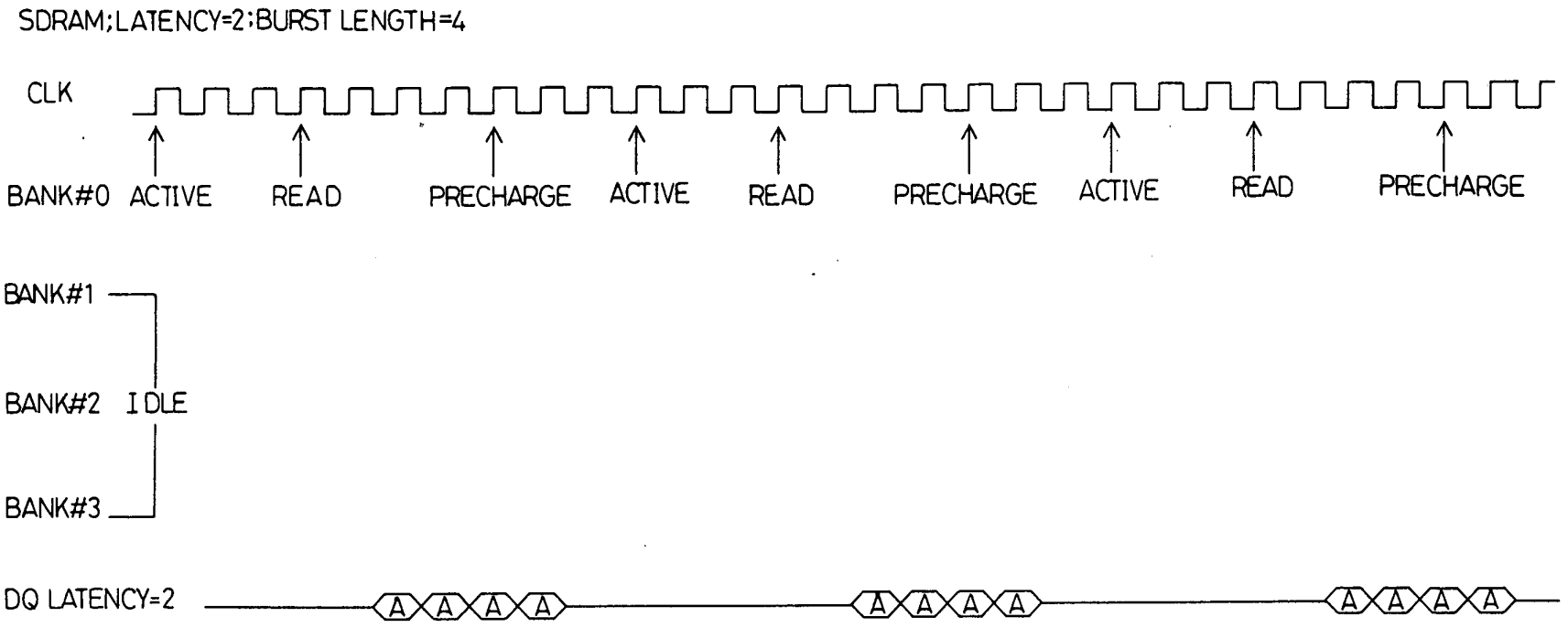

FIG.6A
PRIOR ART

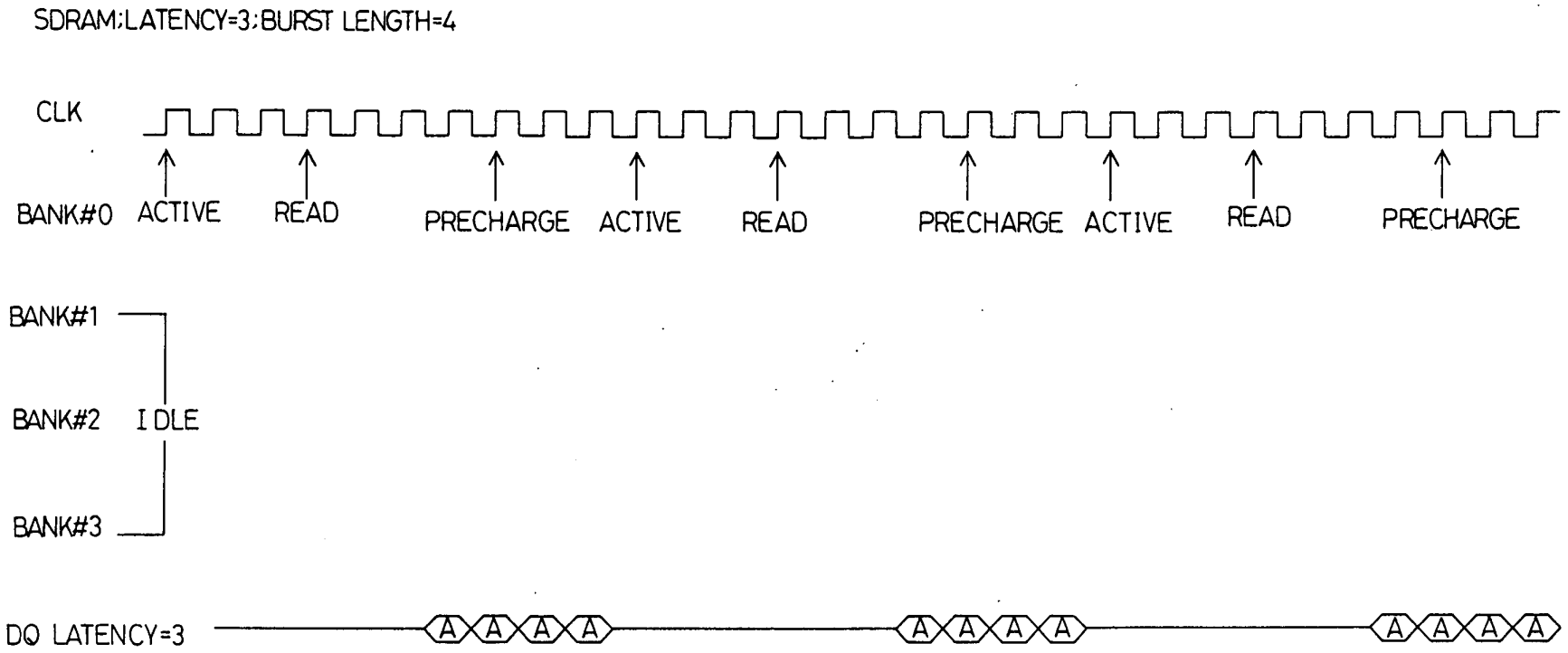

FIG.6B
PRIOR ART

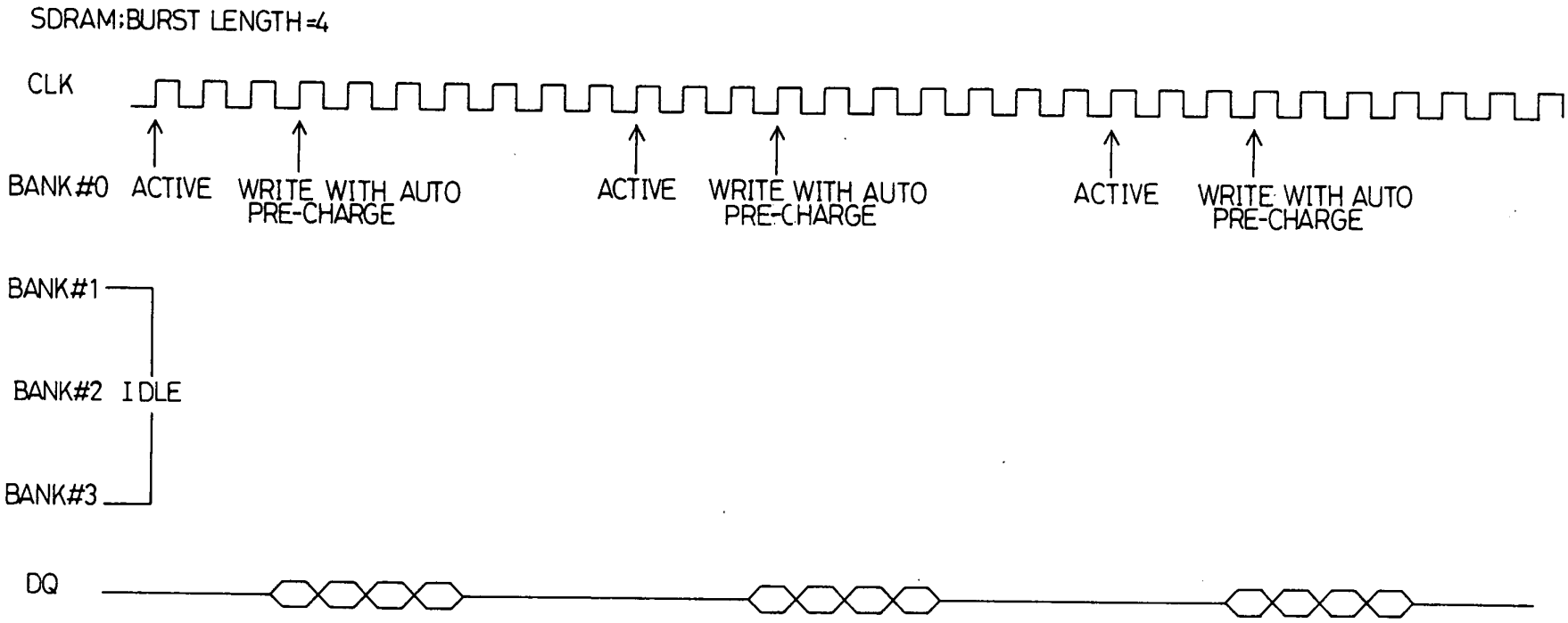

FIG.7
PRIOR ART

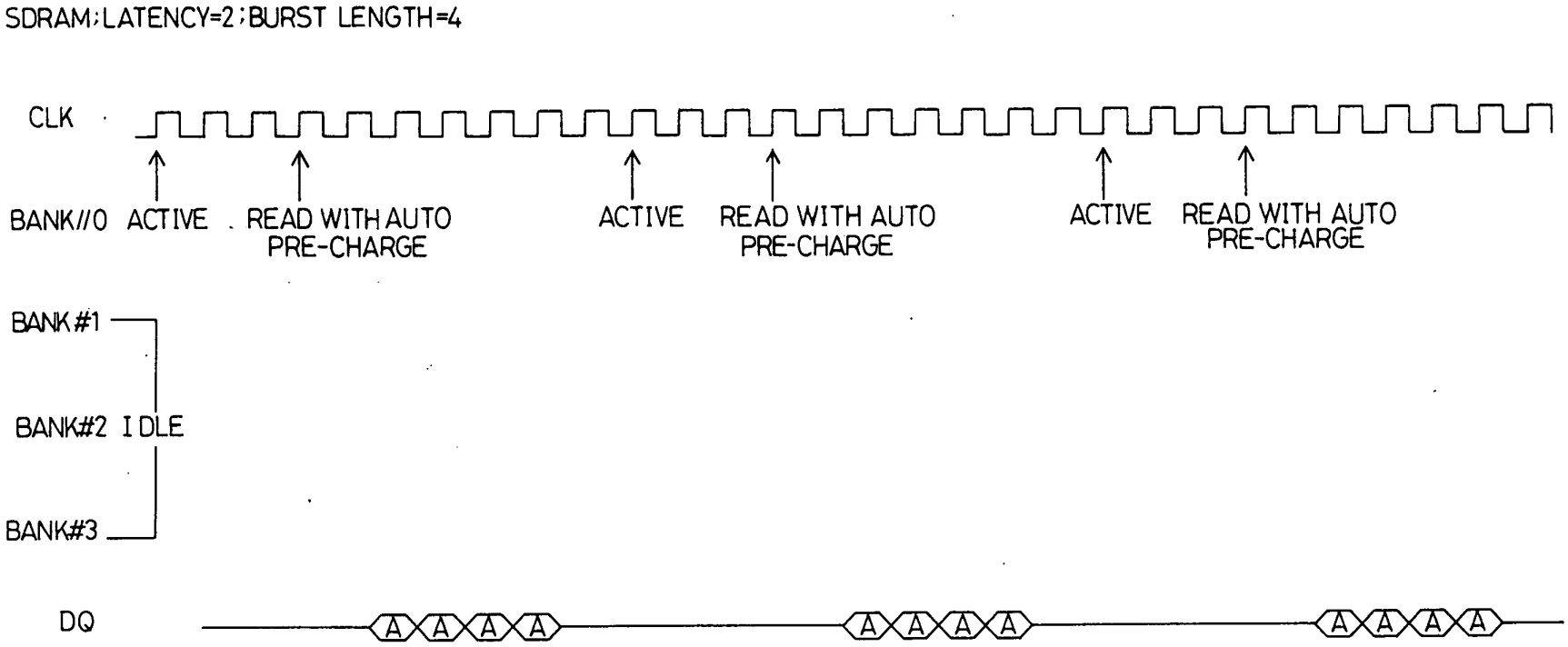

FIG. 8A
PRIOR ART

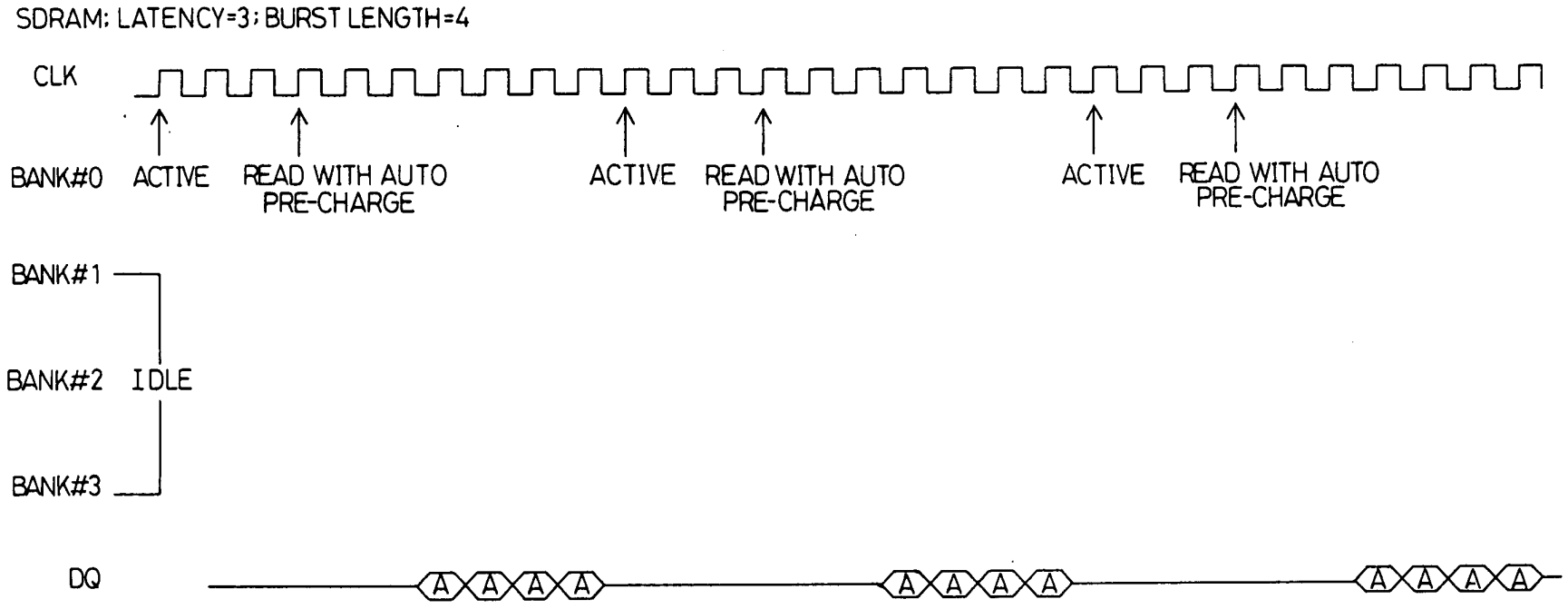

FIG.8B
PRIOR ART

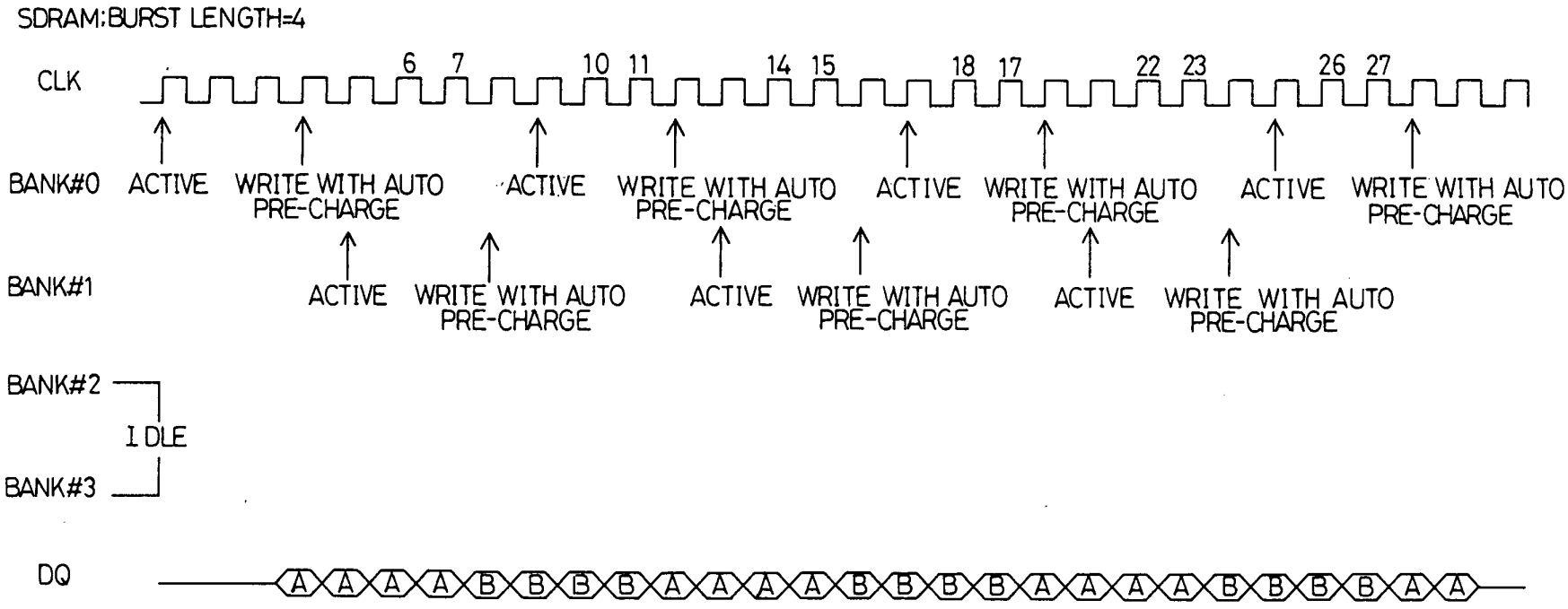

FIG. 9
PRIOR ART

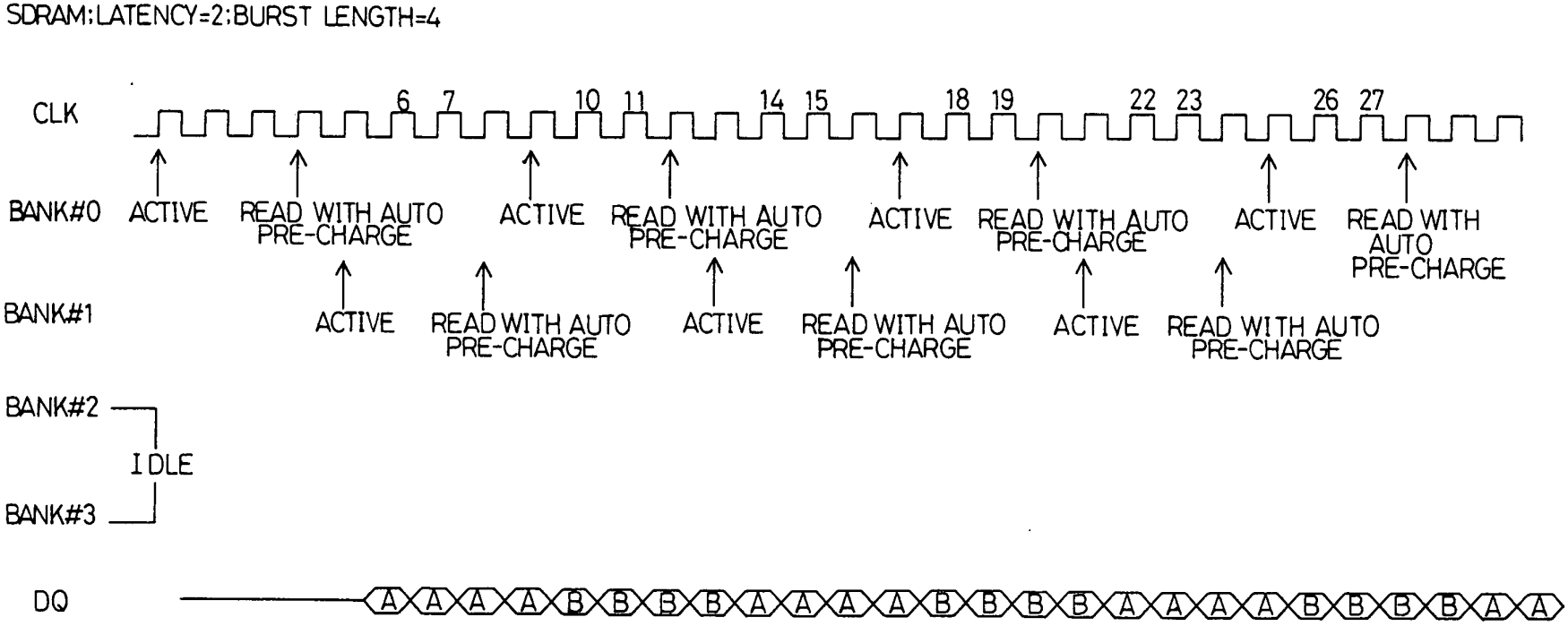

FIG.10A
PRIOR ART

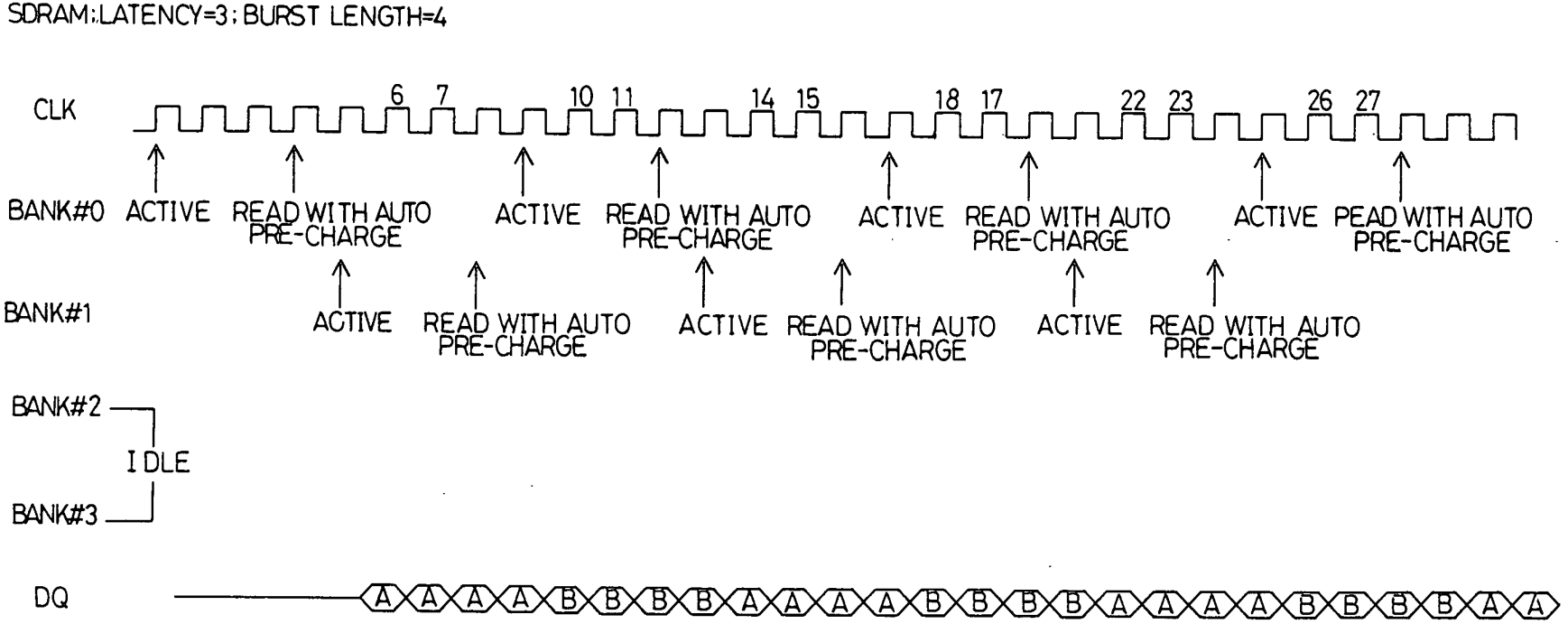

FIG.10B
PRIOR ART

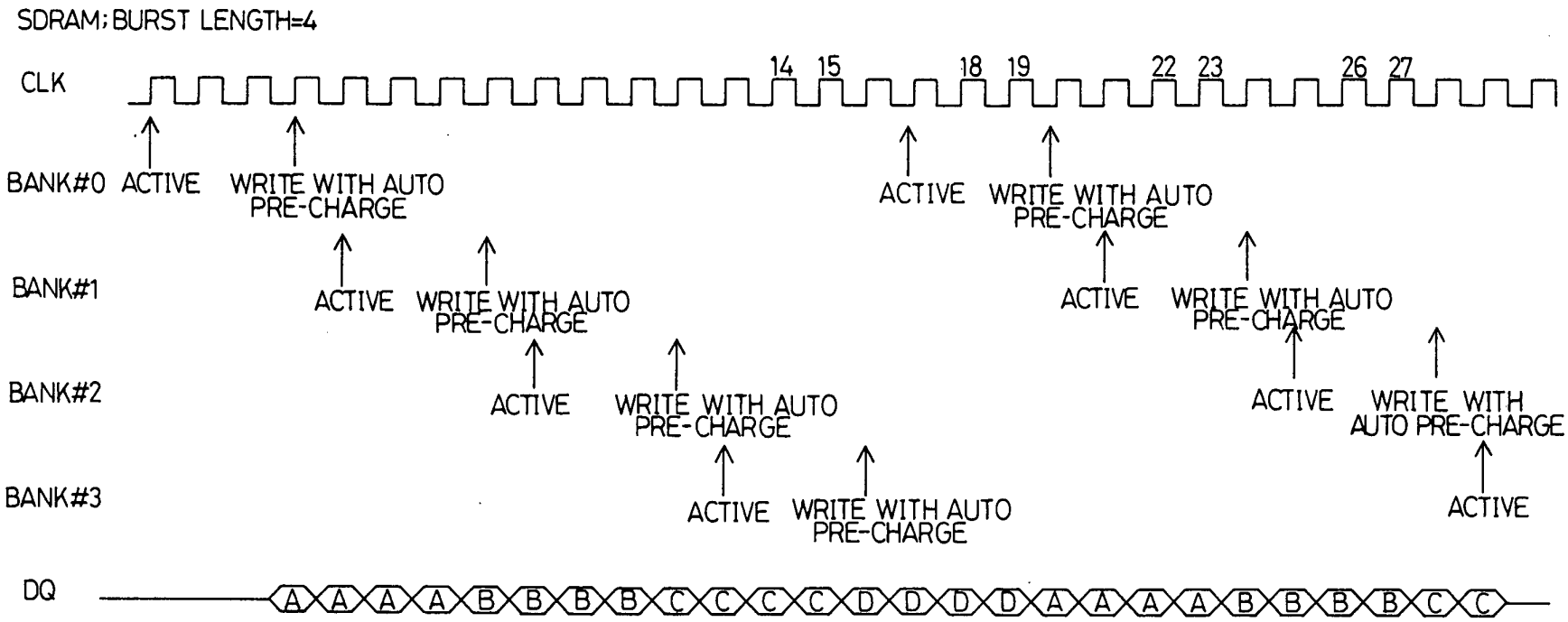

FIG.11
PRIOR ART

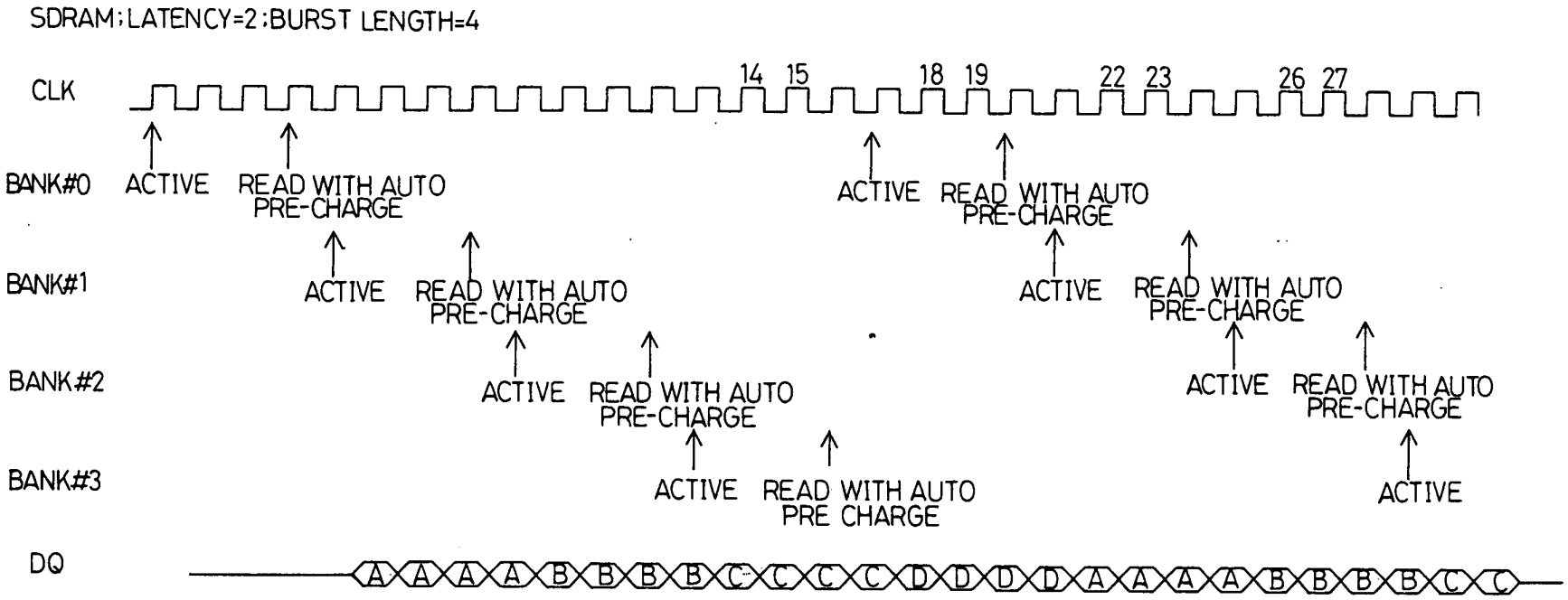

FIG.12A
PRIOR ART

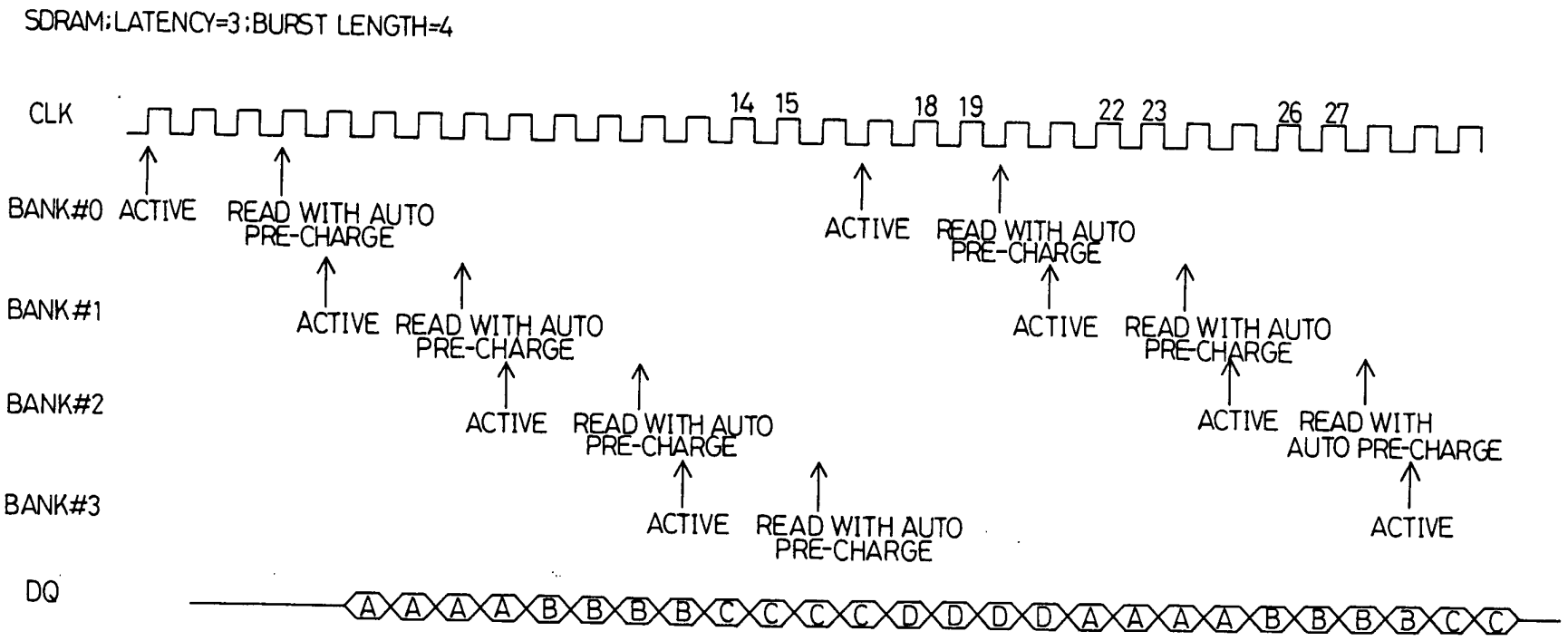

FIG.12B
PRIOR ART